IN THE SPECIFICATION

Please amend the paragraph on page 12 beginning on line 5 as follows:

Referring to Figure 2, a bus hierarchy 60 may include a plurality of buses 64, 74, 86, linked together by bridges 68, 78. This example of a bus hierarchy 60 is only one example of many possible arrangements that may be present in a computer system and is simply used to illustrate the arbitration that occurs between devices and buses in a computer system. A local bus 64 may have a very fast data throughput, although it may support very few devices, such as, for example, a processor 12 and level-2 cache 66, in order to achieve a high level of performance. A bridge 68 may be operably connected to the bus 64 and may arbitrate exchanges of data between the bus 64, main memory (RAM) 20, an AGP bus 70 and a port 72, and an expansion bus 74, such as a PCI bus 74. The bridge 68 may also contain buffers used to reconcile differences in clock speeds between the PCI bus 74 and the local bus 64.

Please amend the paragraph on page 17 beginning on line 4 as follows:

Referring to Figures 8 and 9, an I/O device driver architecture 130 may include an initialization function 132 [and],synchronous functions 134 used to control a synchronous I/O device 90, and return functions 136. The initialization function 132 may initialize any interrupts that the I/O controller 88 may generate in response to conditions such as I/O completion, transfer errors, or the like. In addition, the initialization function 132 may install an interrupt service routine 138 to be executed when an interrupt occurs. The interrupt service routine 138 may then execute asynchronous functions 140 corresponding to the CPU 12 or other asynchronous devices. Once the interrupt service routine 138 responds to an interrupt, control may be returned 142 back to the point of execution interruption.

Please amend the paragraph on page 19 beginning on line 14 as follows:

If the test 162 determines that the operation is a write operation, then a test 166 may check 166 to determine if data is requested by a device from the buffer 112. If data is requested, then a byte of data may be written 170 from the buffer 112, the "transfer count" may be incremented 172, and the process may cycle back up to the test 162.